

DS3100DK Stratum 3/E3 Timing Card IC Demo Kit

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GENERAL DESCRIPTION

The DS3100DK is an easy-to-use demo and evaluation kit for the DS3100 Stratum 3/3E timing card IC. A surface-mounted DS3100 and careful layout provide maximum signal integrity. An on-board Dallas 8051-compatible microcontroller and included software give point-and-click access to configuration and status registers from a personal computer. LEDs on the board indicate interrupt, power-supply function, and GPIO status. The board provides BNC and bantam connectors for the composite clock and BITS interfaces. Single-ended and LVDS clocks are accessed via SMB connectors. All LEDs and connectors are clearly labeled with silkscreening to identify associated signals.

DEMO KIT CONTENTS

DS3100DK PCB

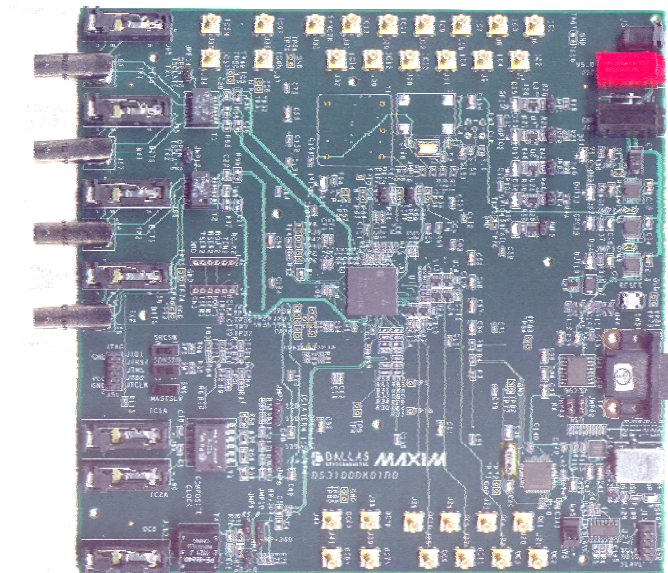
CD_ROM Includes:

DS3100 Software

DS3100 Initialization File

DS3100DK Data Sheet

DS3100 Data Sheet/Errata Sheet



FEATURES

- Soldered DS3100 for Best Signal Integrity
- SMB Connectors, BNC, Bantam, Transformers, and Termination Ease Connectivity
- Careful Layout for Analog Signal Paths
- On-Board Stratum 3 Oscillator with Footprints for Stratum 3E Oscillators
- DS3100 Configured for CPU Bus Operation for Complete Control Over the Device
- On-Board Dallas Microcontroller and Included Software Provide Point-and-Click Access to the DS3100 Register Set
- LEDs for Interrupt, Power Supplies, and GPIO
- Included International Power Supply
- Banana Jack VDD and GND Connectors Support Use of Lab Power Supplies
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers and LEDs
- Header Provided for Master/Slave Connection to a Second DS3100DK
- Software Provides GUI Fields for Most Commonly Used Features Plus Full Read/Write Access to the Entire Register Set
- Software Support for Creating and Running Configuration Scripts Saves Time During Evaluation

MINIMUM SYSTEM REQUIREMENTS

- PC Running Windows® XP or Windows 2000
- Display with 1024 x 768 Resolution or Higher
- Available Serial (COM) Port
- DB-9 Serial Cable

ORDERING INFORMATION

PART	DESCRIPTION
DS3100DK	Demo kit for DS3100

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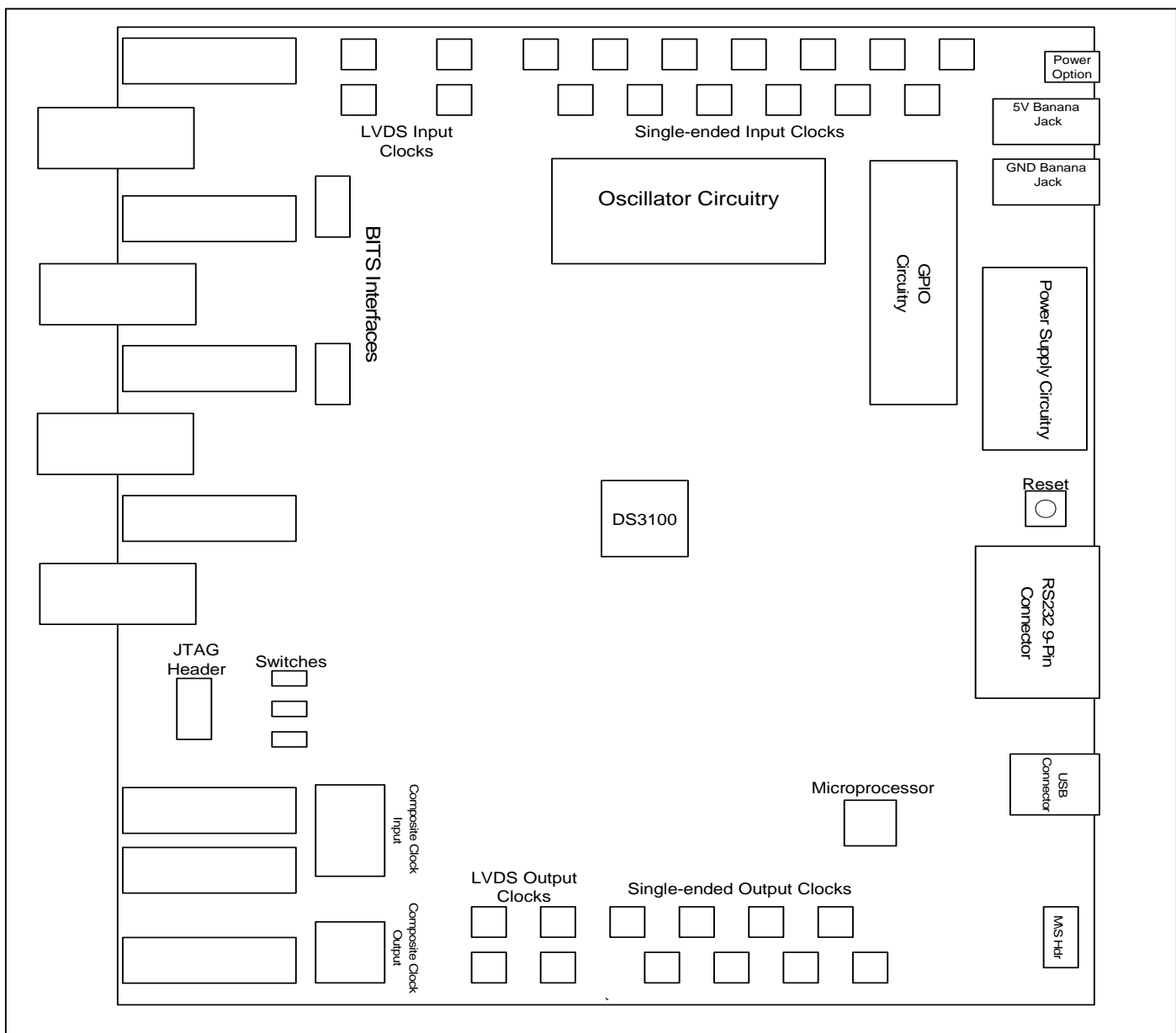
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1. BOARD FLOORPLAN

[Figure 1-1](#) shows the floorplan of the DS3100DK. The DS3100 is in the center of the board, input clock SMB connectors are along the top edge of the board, and output clock connectors are on the bottom edge. Between the input clock connectors and the DS3100, land patterns are provided for several different types of local oscillators, ranging from tiny, inexpensive TCXOs to larger, high-performance OCXOs. The right edge contains, from top to bottom, power supply connectors, DC-DC converters and power-indicator LEDs, reset push-button, serial connector and USB connector. An on-board DS87C520 microcontroller is located near the USB connector. The left edge of the board is occupied by connectors and transformers for the DS3100's built-in BITS (DS1/E1/2048kHz) and composite clock (64kHz) receivers and transmitters. Between the BITS and composite clock connectors are a JTAG header and three switches to control the DS3100's MASTSLV, SONSDH, and SRC5W pins.

See [APPENDIX 1: HARDWARE COMPONENTS](#) for a complete component list. Complete board schematics follow Appendix 2.

Figure 1-1. Board Floorplan



1.1 Input and Output Clocks

There are 13 SMB connectors at the top of the board labeled IC1–IC4, IC7–IC14, and SYNC2K that provide a single-ended clock input to the DS3100. All single-ended clock inputs are connected to the DS3100 with a 50 Ω characteristic impedance trace and terminated with 50 Ω at the device. Four additional SMB connectors labeled IC5P, IC5N, IC6P, and IC6N provide differential clock inputs to the DS3100. These differential inputs have 50 Ω trace impedance and 50 Ω termination at the device (i.e., 100 Ω differential).

On the other end of the PCB are eight SMB clock output connectors labeled OC1–OC5 and OC9, OC10, and OC11. All single-ended clock outputs are buffered at the DS3100 and connected to the SMB connector via a 50 Ω characteristic impedance trace. Four additional SMB connectors labeled OC6P, OC6N, OC7P, and OC7N provide connections to the differential outputs from the DS3100.

1.2 Jumpers, Headers, and Switch Settings

Jumpers JMP1 to JMP4 (upper right of board) provide input settings to the four DS3100 GPIO pins. If a jumper is installed the corresponding GPIO input is high. With no jumper the GPIO pin defaults low. LEDs DS5–DS8 indicate the logic level of the GPIO pins (LED lit means GPIO pin is high). Switches SW7 to SW9 set the SONSDH, SRC5W and MASTSLV pins, respectively, high or low as indicated by the silkscreen. Headers J1 and J2 provide access to BITS1 and BITS2 framer signals, respectively. Header J51 provides access to the JTAG port of the DS3100. Header J15 provides interface to a master or slave board depending on position of switch SW6.

1.3 Composite Clock Interface

Bantam jacks J89 and J90 provide access to composite clock inputs IC1A and IC2A through a 2:1 transformer. Jumpers JMP7 and JMP6 configure termination for IC1A and IC2A respectively. Silkscreen text indicates which jumper is necessary to set the interface at 110 Ω , 120 Ω , or 133 Ω . Bantam jack J117 provides an interface through a 1:1 transformer to the OC8 composite clock output. Jumpers JMP8, JMP9, and JMP10 provide different attenuation configurations that are represented in silkscreen ($R_s = 91\Omega$ with no jumper installed). See the schematics for additional details on the composite clock termination circuitry.

1.4 BITS Interfaces

The BITS1 DS1/E1 LIU uses bantam connectors J85 and J55 or BNC connectors J83 and J57 for transmit and receive interfaces, respectively. The BITS2 LIU uses bantam connectors J86 and J56 or BNC connectors J84 and J58 for transmit and receive, respectively. There is a dual transformer package for each BITS transceiver (component T1 for BITS1 and T2 for BITS2). See the schematics for additional details on the BITS termination circuitry.

1.5 Microcontroller

The DS87C520 microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port or USB port into register accesses on the DS3100. When the microcontroller starts up it turns on DS16 to indicate that the controller is working correctly. A pushbutton switch labeled RESET (SW5) at the right middle of the board resets the microcontroller as well as the DS3100.

1.6 Power-Supply Connectors

The included international power supply can be connected to jack J3 to power the board or a 5V lab power supply can be connected across the red (J13) and black (J19) banana jacks. The 5V input is then regulated to 3.3V and 1.8V and distributed to board components.

2. BASIC HARDWARE SETUP

The following steps provide a quick start to using the DS3100DK.

- 1) Configure the board for serial (RS-232) communication by placing jumpers to connect the left and middle pins of JMP62 and JMP63 (near the serial connector). USB operation is not yet supported.
- 2) Ensure switch SW6 (near the OC1 and OC2 connectors) is in the “MAS” position.
- 3) Set switch SW9 (MASTSLV) in the “1” (master) position.
- 4) Set switch SW8 in “0” (normal operation) position.
- 5) Set switch SW7 to “1” to have the 1.544/2.048MHz frequency options in the DS3100 default to 1.544MHz. Set SW7 to “0” for 2.048MHz.
- 6) Connect a standard DB-9 serial cable between the serial port connector on the DS3100DK and an available serial port on the host computer. (Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.)
- 7) Attach the appropriate AC power supply prongs to the included international power supply.
- 8) Plug the power supply into an AC power outlet and connect the DC output of the supply to connector J3 (PWR in [Figure 1-1](#)).

At this point the power indicator LEDs DS1–DS4 should be lit. Microcontroller status LED DS16 (to the right of the USB connector) should also be lit.

3. INSTALLING AND RUNNING THE SOFTWARE

At this time the DS3100 demo kit software only runs on Windows 2000 or Windows XP operating systems.

To install the demo kit software, run SETUP.EXE from the disk included in the DS3100DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS3100DK.

After software installation is complete, set up the hardware as described above and run the software by double-clicking the *DS3100 Demo Kit* icon on the Windows desktop or by selecting **Start**→**Programs**→**Dallas Semiconductor**→**DS3100 Demo Kit**. When the main window appears, select the correct serial port in the box in the lower right corner. When communication has been properly established between the software and the hardware, the ID field in the upper-left corner should indicate *3100 rev x*, where $x = 0$ for a revision A1 device, and $x = 1$ for a revision A2 device.

The demo kit software always starts in demo mode (with the DEMO MODE checkbox in the upper-left corner checked) in case a user wants to look at the software without having the DK hardware connected to the PC. To connect the software with the demo kit hardware, uncheck the DEMO MODE box. The software optionally initializes the DS3100 device and then reads the state of the device to get ready for use.

3.1 Command Line Options

The demo kit software has these command line options:

-l <filepath>	specifies an alternate log file	example: “DS3100DK.exe -l mylog.mfg
-p[port#]	sets the serial (COM) port number	example: “DS3100DK.exe -p2” sets COM2

To add command line options to a shortcut, such as the DS3100 demo kit shortcut that the installer adds to the desktop, right click on the shortcut and select **Properties**. In the **Shortcut** tab, at the end of the text in the **Target** textbox, add a space followed by the command line option.

4. OVERVIEW OF THE SOFTWARE INTERFACE

4.1 Global Configuration

In the upper-left corner of the main window are several global status and configuration fields including the device ID and REV, the status of the MASTSLV pin (MCR3:MASTSLV), the software DEMO MODE check box, and the 1.544MHz vs. 2.048MHz frequency selection bit (MCR3:SONSDH).

4.2 Input Clock Monitor, Divider, and Selector

This box occupying the left-center section of the main window contains the most frequently used configuration and status associated with input clocks IC1–IC14. At the far left, inputs IC1 and IC2 can be configured for either composite clock (on the IC1A and IC2A pins, respectively) or CMOS (on the IC1 and IC2 pins, respectively). Similarly, IC5 and IC6 can be configured for LVDS or PECL operation.

Just to the right of the input clock numbers 1–14 are software LEDs that indicate the state of each input as reported by its input monitor. These LEDs are red in the absence of any other condition. When a clock of the correct frequency is applied to an input, the associated LED turns yellow when activity is detected and, about 10 seconds later, it turns green if the input clock frequency is within range. If an input is disqualified by one of the DPLLs because the DPLL could not lock to it, the LED turns magenta.

In the middle of the box, the **FREQ** and **LK MODE** fields configure the frequency and lock mode (direct-lock, **DIVN**, or **LOCK8K**) for each input clock. At the bottom is a field to configure the **DIVN** divider used for inputs configured for **DIVN** mode.

All the fields in the box containing the **PRIORITY** fields display information about either the T0 DPLL or the T4 DPLL, depending on which of two radio buttons is selected at the bottom of the box. The **PRIORITY** fields configure the input clock priorities for the selected DPLL. The **SEL REF** field shows the selected reference for the DPLL, while the **REF 1**, **REF 2**, and **REF 3** fields display the three highest priority valid inputs for the DPLL. The **FREQ** and **PHASE** fields show the real-time frequency and phase reported by the DPLL.

In future releases of the DS3100DK software, the **More** button will open a secondary window with additional configuration and status fields.

Table 4-1. Mapping Between Input Clock Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
IC1 Signal Format (CMOS or CC)	MCR5:IC1SF
IC2 Signal Format (CMOS or CC)	MCR5:IC2SF
IC5 Signal Format (LVDS or PECL)	MCR5:IC5SF
IC6 Signal Format (LVDS or PECL)	MCR5:IC6SF
Input Clock Status LEDs	ISR1–ISR7 registers LED red when ACT = 1, HARD = 1 LED yellow when ACT = 0, HARD = 1 LED green when ACT = 0, HARD = 0, LOCK = 0 LED magenta when ACT = 0, HARD = 0, LOCK = 1
FREQ	ICR1–ICR14, FREQ [3:0]
LK MODE	ICR1–ICR14, LOCK8K , and DIVN
PRIORITY	IPR1–IPR7
SEL REF	PTAB1:SELREF
REF 1	PTAB1:REF1
REF 2	PTAB2:REF2
REF 3	PTAB3:REF3
FREQ (ppm)	FREQ 1, FREQ 2 and FREQ 3 registers concatenated
PHASE (deg)	PHASE 1 and PHASE 2 register concatenated

4.3 T0 DPLL

The state of the T0 DPLL (free-run, locked, holdover, etc.) is shown in the STATE field. The STATE CHG, SRFAIL and PHMON fields are buttons that represent latched status bits in the device. When the button is raised in the middle, the corresponding latched status bit has been set in the DS3100. Pressing the button clears the latched status bit. STATE CHG indicates the state of the T0 DPLL has changed since the last time the button was pressed. SRFAIL indicates the selected reference has failed since the last time the button was pressed. PHMON indicates the phase monitor limit (set by PMLIM) has been exceeded.

The state of the T0 DPLL can be forced using the combo box to the left of the STATE field, and the selected reference can be forced using the CLK SEL field. Below the CLK SEL field is a field that configures the T0 DPLL for revertive or nonrevertive input reference switching.

The frequency of the T0 DPLL is displayed in the FREQ field (fixed at 77.76MHz for the DS3100 T0 DPLL). The acquisition and locked bandwidths are set by the ABW and LBW fields, respectively, and the damping factor is set by the DAMP field. The acquisition bandwidth is only used if AUTOBW is checked. If the frequency of the T0 DPLL's selected reference exceeds the SOFT LIMIT setting (in the DPLL FREQUENCY LIMITS box at the top of the window), the SOFTLIM LED turns red.

The PALARM status LED and the PHASE MONITOR and BUILDOUT fields are advanced topics. See [Table 4-2](#) and the DS3100 data sheet for more details.

In future releases of the DS3100DK software, the More button will open a secondary window with additional configuration and status fields.

Table 4-2. Mapping Between T0 DPLL Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
STATE combo box	MCR1:T0STATE
STATE status box	OPSTATE:T0STATE
CLK SEL	MCR2:T0FORCE
Revertive/Nonrevertive	MCR3:REVERT
FREQ	Fixed by T0 DPLL architecture
ABW	T0ABW
LBW	T0LBW
DAMP	T0CR2:DAMP
STATE CHG	MSR2:STATE
SRFAIL	MSR2:SRFAIL
PHMON	MSR3:PHMON
PALARM	TEST1:PALARM
SOFTLIM	OPSTATE:T0SOFT
AUTOBW	MCR9:AUTOBW
LIMINT	MCR9:LIMINT
PMLIM	PHMON:PMLIM
PMEN	PHMON:PMEN
PMPBEN	PHMON:PMPBEN
PBOEN	MCR10:PBOEN
PBOFRZ	MCR10:PBOFRZ
RECAL	FSCR3:RECAL
MANUAL PBO	OFFSET1 and OFFSET2

4.4 T4 DPLL

The state of the T4 DPLL (locked or not locked) is shown in the STATE field. The LOCK and NO INPUT fields are buttons that represent latched status bits in the device. When the button is raised in the middle, the corresponding latched status bit has been set in the DS3100. Pressing the button clears the latched status bit. LOCK indicates the state of the T4 DPLL has changed since the last time the button was pressed. NO INPUT means the T4 DPLL has no valid inputs available. The selected reference for the T4 DPLL can be forced using the CLK SEL field.

The frequency of the T4 DPLL is displayed in the FREQ field. When the FREQ field is changed, the frequency of the T4 option listed in the T4 APLL combo box automatically changes to match. If the T4 option in the T4 APLL box is currently selected, the frequencies of all of the T4 options in the OC1–OC7 output clock combo boxes automatically change to frequencies derived from the new T4 APLL frequency. These changes match what happens inside the DS3100 device.

The bandwidth of the T4 DPLL is set by the BW field, while the damping factor is set by the DAMP field. If the frequency of the T4 DPLL's selected reference exceeds the SOFT LIMIT setting (in the DPLL FREQUENCY LIMITS box at the top of the window), the SOFTLIM LED turns red. Digital feedback (vs. analog feedback through the T4 APLL) can be selected using the DIGFB checkbox.

The LKT4T0 and T4MT0 fields are advanced topics. See [Table 4-3](#) and the DS3100 data sheet for more details.

In future releases of the DS3100DK software, the More button will open a secondary window with additional configuration and status fields.

Table 4-3. Mapping Between T4 DPLL Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
STATE	OPSTATE:T4LOCK
CLK SEL	MCR4:T4FORCE
FREQ	T4CR1:T4FREQ
BW	T4BW
DAMP	T4CR2:DAMP
LOCK	MSR3:T4LOCK
NO INPUT	MSR3:T4NOIN
SOFTLIM	OPSTATE:T4SOFT
DIGFB	MCR4:T4DFB
LKT4T0	MCR4:LKT4T0
T4MT0	T0CR1:T4MT0

4.5 T0 APLL

The T0 APLL can be connected to the output of the T0 Output DFS or to the T0 Low-Frequency DFS (see DS3100 data sheet for details). The frequency options listed in the T0 APLL field are all APLL *input* frequencies. The APLL *output* frequency is always four times the input frequency. The difference between the “77.76 Analog” and “77.76 Digital” options is whether or not the feedback path of the T0 DPLL includes the T0 feedback APLL. The non-77.76 options in the T0 APLL field are all frequencies from the T0 Low-Frequency DFS. When the T0 APLL setting is changed, the frequencies of all the T0 options in the OC1–OC7 output clock combo boxes automatically change to frequencies derived from the new T0 APLL frequency. These changes match what happens inside the DS3100 device.

Table 4-4. Mapping Between T0 APLL Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
T0 APLL	T0CR1:T0FREQ

4.6 T4 APLL

The T4 APLL can be connected to the output of the T4 DPLL or to the output of the T0 DPLL (specifically the T0 low-frequency DFS; see DS3100 data sheet for details). The frequency options listed in the T4 APLL field are all APLL *input* frequencies. The APLL *output* frequency is always four times the input frequency.

When the FREQ field is changed in the T4 DPLL box, the frequency of the T4 option listed in the T4 APLL combo box automatically changes to match. If the T4 option in the T4 APLL box is currently selected, the frequencies of all the T4 options in the OC1–OC7 output clock combo boxes automatically change to frequencies derived from the new T4 APLL frequency. These changes match what happens inside the DS3100 device. Similarly, if the T4 APLL option is changed, the frequencies of all the T4 options in the OC1–OC7 output clock combo boxes automatic change to frequencies derived from the new T4 APLL frequency.

Table 4-5. Mapping Between T4 APLL Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
T4 APLL	T0CR1:T4APT0, T0CR1:T0FT4

4.7 Output Clocks

The fields in this box configure the DS3100's 11 output clocks. The 2K8K field specifies the source (T0 path or T4 path) for the 2kHz and 8kHz clock options for output clocks OC1–OC7. Similarly the DIG1 and DIG2 fields configure the Digital1 and Digital2 frequency options for OC1–OC7 (see the DS3100 data sheet for details).

The OC1–OC7 fields specify the output frequencies for outputs OC1–OC7. Note that when the T0 APLL setting is changed, the frequencies of all the T0 options in the OC1–OC7 fields automatically change to frequencies derived from the new T0 APLL frequency. Similarly, when the T4 APLL setting is changed, the frequencies of all the T4 options in the OC1–OC7 fields automatically change to frequencies derived from the new T4 APLL frequency. These changes match what happens inside the DS3100 device.

The OC89 field specifies whether the T0 path or the T4 path is the source for output clocks OC8 and OC9. OC8 is the 64kHz composite clock output. The OC8 field configures the OC8 output clock for 50% or 5/8 duty cycle, and also for whether or not the output signal has 8kHz BPVs and optionally 400Hz absence-of-BPVs per ITU-T G.703 Appendix II options a) and b). The “8K” options in the list enable the 8kHz BPVs but not the 400Hz absence-of-BPVs. The “400” options enable both the 8kHz BPVs and the 400Hz absence-of-BPVs. OC9 is a dedicated 1.544MHz or 2.048MHz output. When OC89 specifies that OC8 and OC9 are sourced from the T4 path, the Auto Squelch checkbox specifies whether or not OC8 and OC9 are automatically squelched when T4 has no valid input references. When OC89 indicates T0 path, Auto Squelch is not available to match DS3100 behavior.

OC10 is an 8kHz output that can be configured as a 50% duty cycle clock or a frame pulse and can optionally be inverted. OC11 is a 2kHz output that can be similarly configured.

Table 4-6. Mapping Between Output Clock Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
2K8K	FSCR1:2K8KSR
DIG1	MCR6:DIG1SS, MCR7:DIG1F
DIG2	MCR6:DIG2SS, MCR7:DIG2F, MCR7:DIG2AF
OC1–OC7	OCR1–OCR4
OC89	MCR4:OC89
Auto Squelch	T4CR1:ASQUEL
OC8	OCR4:OC8EN, T4CR1:OC8DUTY MCR8:OC8NO8, MCR8:OC8400
OC9	OCR4:OC9EN, T4CR1:OC9SON
OC10	OCR4:OC10EN, FSCR1:8KPUL, FSCR1:8KINV
OC11	OCR4:OC11EN, FSCR1:2KPUL, FSCR1:2KINV

4.8 DPLL Frequency Limits, Phase Detectors, DPLL Lock Criteria

The DPLL frequency limits specify the hard and soft limits of the DPLL frequency range. When the selected reference for a DPLL exceeds the soft limit, the SOFTLIM LED for that DPLL turns red but the selected reference is not disqualified. If the FLLLOL (frequency limit loss of lock) box is checked in the DPLL Lock Criteria box, when the selected reference for a DPLL exceeds the hard limit the DPLL will lose lock (T4 transitions to Not Locked state, and T0 transitions to LOL state).

The remaining fields are advanced topics. See [Table 4-7](#) and the DS3100 data sheet for more details.

Table 4-7. Mapping Between DPLL Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
HARD LIMIT	HARDLIM[9:0] in DLIMIT1 and DLIMIT2
SOFT LIMIT	DLIMIT3:SOFTLIM
MCPDEN	PHLIM2:MCPDEN
USEMCPD	PHLIM2:USEMCPD
D180	TEST1:D180
COURSELIM	PHLIM2:COARSELIM
FINELIM	PHLIM1:FINELIM
FLEN	PHLIM1:FLEN
CLEN	PHLIM2:CLEN
FLLLOL	DLIMIT3:FLLLOL
NALOL	PHLIM1:NALOL

4.9 BITS Receivers and BITS Transmitters

The Mode fields in these boxes set the basic line mode for each port (DS1 ESF or SF, E1, 2048kHz, and—for receivers only—6312kHz). The termination fields specify the line termination for the receiver or transmitter port. The DS3100 supports either internal termination (inside the device) or external termination (resistors on the board). As shipped from the factory the demo kit hardware does not have external termination resistors populated, and therefore only the internal termination options should be selected in the software. The input clock (IC1–IC14) to which each BITS receiver should be connected is specified in the CLOCK DEST fields. The output clock to which each BITS transmitter should be connected is specified in the CLOCK SOURCE fields.

In the BITS Transmitters box, when a transmitter is in DS1 ESF or E1 mode, the SSM value to be transmitted can be specified in the SSM fields below the TX1 and TX2 headings. In E1 mode, the Sa bit channel in which to transmit SSMs can be specified (for both transmitters) in the small combo box next to the SSM label.

In the BITS Receivers box, when a receiver is in DS1 ESF or E1 mode, the received SSM values are displayed in the SSM fields below the RX1 and RX2 headings. In E1 mode, the Sa channel in which to look for incoming SSMs can be specified (for both receivers) in the small combo box next to the SSM label.

In future releases of the DS3100DK software, the headings RX1, RX2, TX1, and TX2 will also be buttons that open secondary windows with additional configuration and status fields.

4.9.1 Note About Working with the BITS Receivers and Transmitters

- 1) When switching BITS transmitter or receiver modes, the termination must be changed to match: internal 100Ω for DS1, internal 75Ω or 120Ω for E1 and 2048kHz, internal 75Ω for 6312kHz.
- 2) When switching BITS transmitter modes between DS1 and E1/2048kHz modes, the rate of the transmit clock source (typically OC9) must be changed to match: 1.544MHz for DS1 and 2.048MHz for E1/2048kHz.
- 3) Enabling analog loopback between BITS transmitter 1 and BITS receiver 1 and between BITS transmitter 2 and BITS receiver 2 can be useful in evaluating the DS3100. During device initialization the DS3100DK software enables analog loopback for both BITS transmitter/receiver pairs by setting ALB = 1 in registers B1BLCR4 (address 93h) and B2BLCR4 (address 113h).

Table 4-8. Mapping Between BITS Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
BITS RECEIVERS	
Mode	BMCR:RMODE, BCCR3:MCLKFC, BRMMR, BRRCR1:RB8ZS, BRRCR1:RFM, BRRCR3:RHDB3, BRRCR3:RCRC4 See APPENDIX 2: BITS MODE WRITE SEQUENCES for exact write sequences for each mode
Termination	BLCR3:RION, BLCR3:RIMP
Clock Dest	BCCR2:RCLKD
Left-Hand SSM Combo (E1 Only)	BRMCR:SSMCH
SSM Textboxes	DS1 ESF: BTBOC:TBOC E1: BRMSR, BRSSM:SSM
BITS TRANSMITTERS	
Mode	BMCR:TMODE, BTMMR, BTCCR1:TB8ZS, BTCCR3:TFM, BTCCR4:THDB3, BTCCR4:TCRC4, 60, 61 See APPENDIX 2: BITS MODE WRITE SEQUENCES for exact write sequences.
Termination	BLCR2:TION, BLCR2:TIMP
Clock Source	BCCR1:TCLKS
Left-and SSM Combo (E1 Only)	Indicates which of BTSa4–BTSa8 to use
Main SSM Combos	DS1 ESF: BRBOC:RBOC E1: BTSa4–BTSa8

4.10 Composite Clock Receivers

The AMI and LOS fields are buttons that represent latched status bits in the device. When the button is raised in the middle, the corresponding latched status bit has been set in the DS3100. Pressing the button clears the latched status bit. The AMI buttons indicate a deviation from the expected one-BPV-in-eight pattern has occurred since that button was last pressed. The LOS buttons indicate no pulses were detected in the input signal in a 32 μ s period (i.e., after two missing pulses).

In future releases of the DS3100DK software, the **More** button will open a secondary window with additional configuration and status fields.

Table 4-9. Mapping Between CC Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
IC1 AMI	MSR3:AMI1
IC1 LOS	MSR3:LOS1
IC2 AMI	MSR3:AMI2
IC2 LOS	MSR3:LOS2

4.11 REFCLK Calibration

Any known frequency error in the local oscillator can be calibrated out inside the DS3100 by setting the ppm value in the REFCLK box. Also the significant edge of the REFCLK signal can be selected in XOEDGE field.

Table 4-10. Mapping Between REFCLK Software Fields and DS3100 Register Fields

SOFTWARE FIELD	DS3100 REGISTER FIELDS
REFCLK slider/textbox	MCLKFREQ[15:0] in MCLK1 and MCLK2
XOEDGE	MCR3:XOEDGE

4.12 Register View Window

When the Register View button in the upper-right corner of the main window is pressed, the Register View window appears. In this window the DS3100's entire register set can be viewed and manually written as needed.

The large grid that takes up most of the window displays the DS3100 register map. For each register, its hexadecimal address in square brackets is followed by its register name and its contents in 2-digit hex format. The DS3100's core register space is 00h to 7Fh, its BITS transceiver 1 register space is 80h to FFh, and its BITS transceiver 2 register space is 100h to 17Fh. To distinguish between BITS1 and BITS2 registers, all BITS1 register names start with "B1" and all BITS2 register names start with "B2."

When a register is clicked on in the main register grid, its register description and fields are displayed at the bottom of the window. Due to the limited speed of the serial port, the demo kit software does not continually poll every register and make real-time updates to the data displayed on the Register View screen. Register of concern should be manually read as described below.

The Register View window supports the following actions:

- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Press the Read All button.
- **Write a register field.** Select the register, double-click the field, and enter the value to be written.
- **Write a register.** Double-click the register name in the register array and enter the value to be written.
- **Write a multi-register field.** Double-click on one of the register names in the register array and enter the value for the field.

The software will not allow writes to read-only registers or fields, but it does allow writes to registers that have a mix of read/write and read-only fields.

4.13 Configuration Scripts and Log File

4.13.1 Configuration Log File

Every write command issued by the software to the DS3100DK board is logged in file DS3100DKLog.mfg located in the same directory as the software executable. This file can be viewed in Notepad by pressing the Log File button in the upper-right corner of the main window. Command line option "-l <filepath>" can be used to cause the software to write to a different file than DS3100DKLog.mfg.

4.13.2 Configuration Scripts

All or part of the text in the Configuration Log File can be copied to a text file with a .mfg file extension for use as a configuration script. Configuration scripts are useful for quickly configuring the DS3100 without having to remember all of the required settings.

Two types of configuration scripts are possible: full and partial. A full configuration script can start with the DS3100 in its power-on default state and configure every aspect of the device to bring it to a desired state. To make a full configuration script, run the software, uncheck the Demo Mode checkbox, configure the device using the DK software fields (including Register View writes as needed), press the Log File button, and use File->Save As in Notepad to save a copy of the entire log file to a different file name.

A partial configuration file only affects a subset of the DS3100 device settings. To make a partial configuration script, press the Log File button to view the Log File, press Ctrl-End to jump to the end of the file, and add to the end of the file a carriage return or comment line (starting with a semicolon) to delimit the start of the configuration. Then save and exit the Log File. Next configure the device using the DK software fields (including Register View writes as needed). Finally view the log file again, jump to the end, and copy everything from the delimiter you made earlier to the end of the file into a new .mfg file.

To run a configuration script, press the Config Script button in the upper-right corner of the main window. In the script window, type the path to the file or press the Browse button to navigate to the file. Note that the browser window does not have Desktop and My Documents at the top of the file hierarchy like Windows XP does. Both Desktop and My Documents for <username> can be found under c:\Documents and Settings\<username>.

Note that when the Demo Mode checkbox is unchecked, during the "Initializing the DS3100" step, the software runs configuration script startup.mfg located in the same directory as the software executable. Startup.mfg can be edited or replaced as needed to change the initial configuration of the device.

5. ADDITIONAL INFORMATION AND RESOURCES

5.1 DS3100 Information

For more information about the DS3100, refer to the DS3100 data sheet at www.maxim-ic.com/DS3100.

5.2 DS3100DK Information

For more information about the DS3100DK including software downloads, refer to the DS3100DK Quick View page at www.maxim-ic.com/DS3100DK.

5.3 Technical Support

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

6. APPENDIX 1: HARDWARE COMPONENTS

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C2, C3, C8, C42, C59–C138, C140, C142, C143, C145, C147, C149, C151, C155, C163–C166, C168, C169	99	0.1 μ F \pm 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C4, C5, C6, C27	4	Ceramic capacitors (0805) DO NOT POPULATE	—	—
C6	1	470pF \pm 5%, 50V CGO ceramic capacitor (0805)	AVX	08055A471JAT
C7	1	68 μ F \pm 20%, 16V tantalum capacitor (D case)	Panasonic	ECS-T1CD686R
C13, C14, C16, C41	4	4.7 μ F \pm 10%, 25V X5R ceramic capacitors (1206)	Panasonic	ECJ-3YB1E475K
C17, C18, C20	3	6.8 μ F \pm 10%, 6.3V X5R ceramic capacitors (1206)	Panasonic	ECJ-3YB0J685K
C28, C29	2	560pF \pm 5%, 50V NPO ceramic capacitor (0805)	Panasonic	ECJ-2VC1H561K
C34–C38, C51–C58, C139, C141, C153, C154	17	10 μ F \pm 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C39, C40	2	22pF \pm 10%, 100V ceramic capacitors (1206)	AVX Corp.	12061A220KAT2A
C43	1	1 μ F \pm 10%, 16V ceramic capacitor (1206)	Panasonic	ECJ-3YB1C105K
C48, C49	2	0.47 μ F \pm 10%, 16V ceramic capacitors (0805)	Panasonic	ECJ-2YB1C474K
D1	1	1A, 50V general-purpose silicon diode	Vishay General Semiconductor	1N4001
D7	1	1A, 40V Schottky diode	International Rectifier	10BQ040
DS1–DS4	4	Green LEDs (SMD)	Panasonic	LN1351C
DS5–DS10	6	Red LEDs (SMD)	Panasonic	LN1251C
DS16	1	Green LED (SMD)	Panasonic	LN1351C
J1, J2	2	6-pin socket strip (single row, vertical)	Samtec	SS-106-TT-2-N
J3	1	2.1mm/5.5mm closed frame power jack, high current (right angle PCB, 24VDC at 5A)	CUI Inc.	PJ-002AH
J6–J12, J20–J41	29	5-pin vertical SMB connectors (50 Ω)	AMP	413990-1
J13	1	Red socket (banana plug, horizontal)	Mouser	164-6219
J14	1	5-pin vertical SMB connector (50 Ω) DO NOT POPULATE	AMP	413990-1
J15	1	10-pin terminal strip (dual row, vertical)	Samtec	TSW-105-07-T-D
J19	1	Black horizontal banana plug socket	Mouser	164-6218
J50	1	DB9 right-angle connector (long case)	AMP	747459-1
J51	1	10-pin terminal strip (dual row, vertical)	—	—
J54	1	USB Type B black connector (right angle)	Molex	67068-0000
J55, J56, J85, J86, J89, J90, J117	7	Bantam jack connectors (right angle)	Switchcraft	RTT34B02
J57, J58, J83, J84	4	5-pin BNC connectors (50 Ω , right angle)	Trompeter	CBJR220

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
JMP1–JMP5, JMP8, JMP9, JMP11, JMP12, JMP36, JMP37	11	2-pin vertical headers, 0.100" centers	Samtec	TSW-102-07-T-S
JMP6, JMP7, JMP10, JMP62, JMP63	5	3-pin vertical headers, 0.100" centers	Samtec	TSW-103-07-T-S
R1	1	10k Ω \pm 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ103V
R2, R3, R6, R7, R9, R11, R16-R18	9	Resistors (0603) DO NOT POPULATE	—	—
R4, R5, R8, R10, R12- R14, R20, R25, R42, R46, R84, R91, R92, R95-R97, R110, R113, R115, R116, R120- R123	25	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R15, R22, R23, R24, R41, R43, R45, R47, R49, R51, R53, R55, R80, R81, R111, R112, R117, R118	18	0 Ω \pm 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R19, R21, R40, R44	4	1.0k Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R26, R27, R48, R50, R52	5	470 Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ471V
R28	1	33.2 Ω \pm 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF33R2V
R29–R35, R59–R68	17	51.1 Ω \pm 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF51R1V
R36–R39, R94, R108	6	330 Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R54, R56, R57, R58, R74, R77, R89, R90	8	0 Ω \pm 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R69, R72	2	110 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF1100V
R70, R93	2	10.0 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF10R0V
R71, R73	2	13.0 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF13R0V
R75, R76	2	90.9 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF90R9V
R78	1	357 Ω \pm 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF3570V
R79	1	301 Ω \pm 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF3010V
R82, R83	2	0.0 Ω \pm 5%, 1/10W resistors (0805)	Panasonic	ERJ-6GEY0R00V
R85–R88	4	Resistors (0805) DO NOT POPULATE	—	—
SW5	1	4-pin single-pole switch	Panasonic	EVQPAE04M
SW6	1	6-pin, through-hole, DPDT slide switch	Tyco	SSA22
SW7, SW8, SW9	3	3-pin, through-hole, SPDT slide switches	Tyco	SSA12
T1, T2	2	16-pin SMT T1 transformers (1CT:1CT and 1CT:2CT, 1500V)	Pulse Engineering	PE-68678
T3	1	12-pin dual SMT transformer (64kbps, 1CT:2CT, 1500V)	Pulse Engineering	T7015
T4	1	64kbps interface transformer (1CT:1CT, 1500V, 6-pin DIP)	Pulse Engineering	PE-65540
TP1–TP10, TP18– TP42, TP49–TP61, TP65–TP84	68	1 plated hole test points DO NOT STUFF	—	—
U1	1	High-frequency, surface-mount socket (1mm, 256-pin BGA)	Ironwood Electronics	SG-BGA-6017
U2, U3, U5, U7, U9–U26	22	TinyLogic ultra-high-speed 2-input OR gates (5-pin SOT23)	Fairchild Semiconductor	NC7SZ32M5

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U4, U6	2	3.3V linear regulator (16-pin TSSOP-EP)	Maxim	MAX1793EUE-33
U8	1	1.8V linear regulator (16-pin TSSOP-EP)	Maxim	MAX1793EUE-18
U27	1	3-line to 8-line decoder/demultiplexer (16-pin SO)	Texas Instruments	SN74HC138NSR
U41	1	Dual RS-232 transmitter/receiver (16-pin, 300-mil SO)	Dallas Semiconductor	DS232AS
U42	1	High-speed microcontroller (44-pin TQFP, 0°C to +70°C)	Dallas Semiconductor	DS87C520-ECL
U44	1	Microprocessor voltage monitor (3.08V reset threshold) (4-pin SOT143)	Maxim	MAX811TEUS-T
U45	1	Microprocessor voltage monitor (4.38V reset threshold) (4-pin SOT143)	Maxim	MAX812MEUS-T
U46	1	Single-chip USB to UART bridge (28-pin QFN)	Silicon Laboratories	CP2101
Y1	1	3.3V, 12.8MHz OCXO (5-pin) through-hole DO NOT POPULATE	Vectron	MC853X4-035W
Y2	1	3.3V, 12.8MHz TCXO (4-pin SMD)	Vectron	C22601A1-0028
Y3	1	3.3V, 12.8MHz OCXO (4-pin SMD) DO NOT POPULATE	Vectron	C4400A1-0044
Y7	1	Low-profile 11.0592MHz crystal	Pletronics	LP49-33-11.0592M

7. APPENDIX 2: BITS MODE WRITE SEQUENCES

BITS Transmitter

DS1 ESF

address 04h, set TMODE[1:0]=00
 address 21h, write 02h
 address 21h, write 00h
 address 27h, write 0Ch
 address 29h, write 00h
 address 21h, write 80h
 address 21h, write C0h

DS1 SF/D4

address 04h, set TMODE[1:0]=00
 address 21h, write 02h
 address 21h, write 00h
 address 27h, write 0Ch
 address 29h, write 04h
 address 21h, write 80h
 address 21h, write C0h

E1

address 04h, set TMODE[1:0]=01
 address 21h, write 02h
 address 21h, write 00h
 address 29h, write 00h
 address 2Ah, write 05h
 address 21h, write 81h
 address 21h, write C1h
 address 60h, write 1Bh
 address 61h, write 40h

2048kHz

address 04h, set TMODE[1:0]=10
 address 21h, write 02h
 address 21h, write 00h

BITS Receiver

DS1 ESF

address 04h, set RMODE[1:0]=00
 address 0Ah, write 40h
 address 20h, write 02h
 address 20h, write 00h
 address 22h, write 40h
 address 20h, write 80h
 address 20h, write C0h

DS1 SF/D4

address 04h, set RMODE[1:0]=00
 address 0Ah, write 40h
 address 20h, write 02h
 address 20h, write 00h
 address 22h, write 60h
 address 20h, write 80h
 address 20h, write C0h

E1

address 04h, set RMODE[1:0]=01
 address 20h, write 02h
 address 20h, write 00h
 address 24h, write 68h
 address 20h, write 81h
 address 20h, write C1h

2048 kHz

address 04h, set RMODE[1:0]=10
 address 20h, write 02h
 address 20h, write 00h

6312 kHz

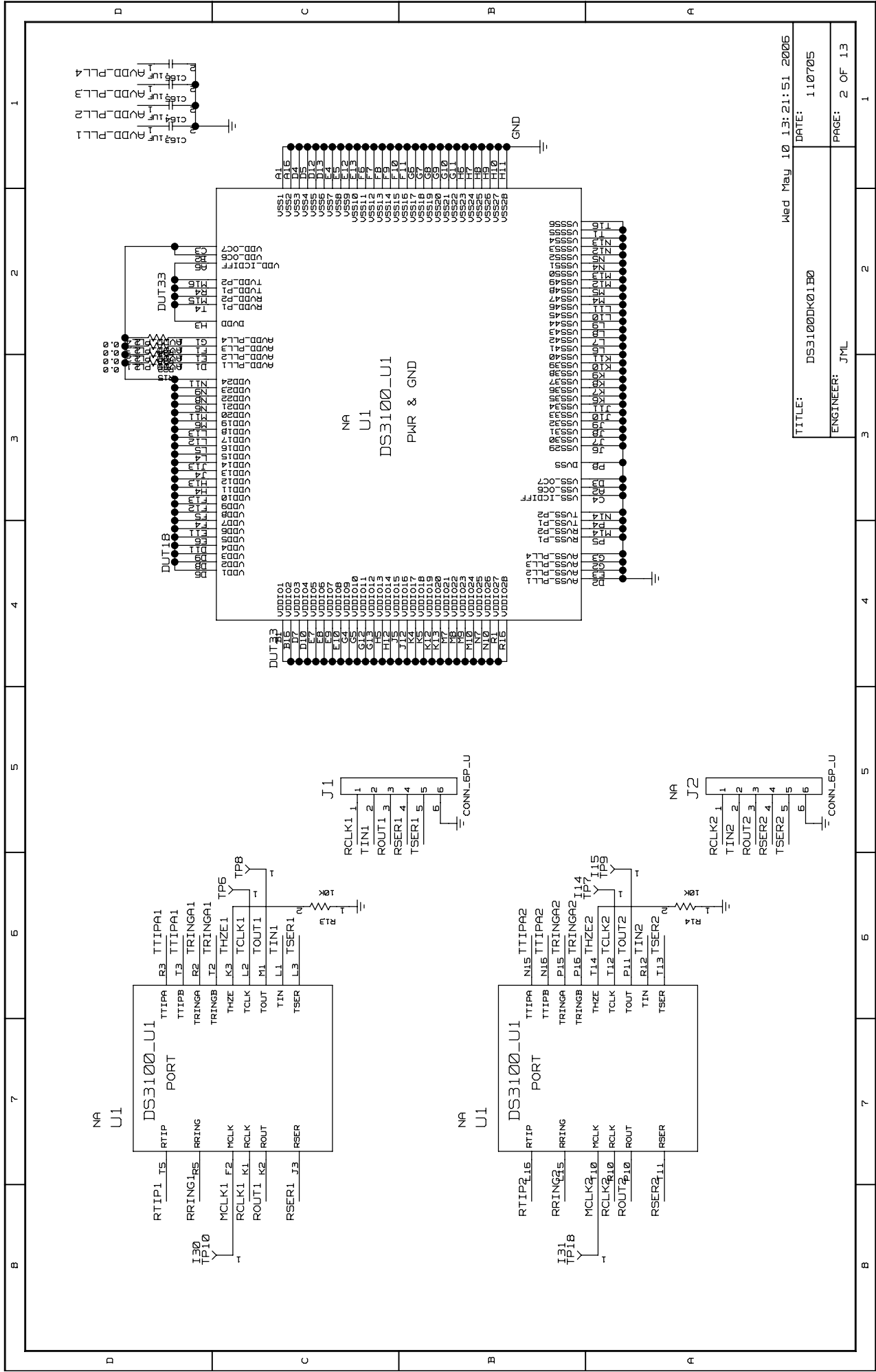
address 04h, set RMODE[1:0]=11
 address 20h, write 02h
 address 20h, write 00h

8. SCHEMATICS

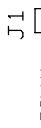
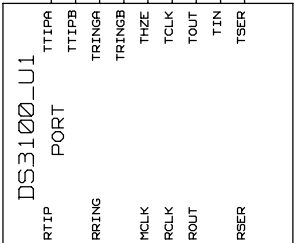
The DS3100DK schematics are featured in the following 13 pages.

9. DOCUMENT REVISION HISTORY

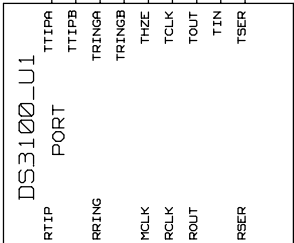
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091806	Initial DS3100DK data sheet release.
110206	Updated document to describe software v0.7 features: (page 1) <i>Features</i> section; (page 6) Section 3.1; (page 14) Section 4.12; (page 15) added Section 4.13, 4.13.1, 4.13.2; updated table captions.



NA
U1



NA
U1



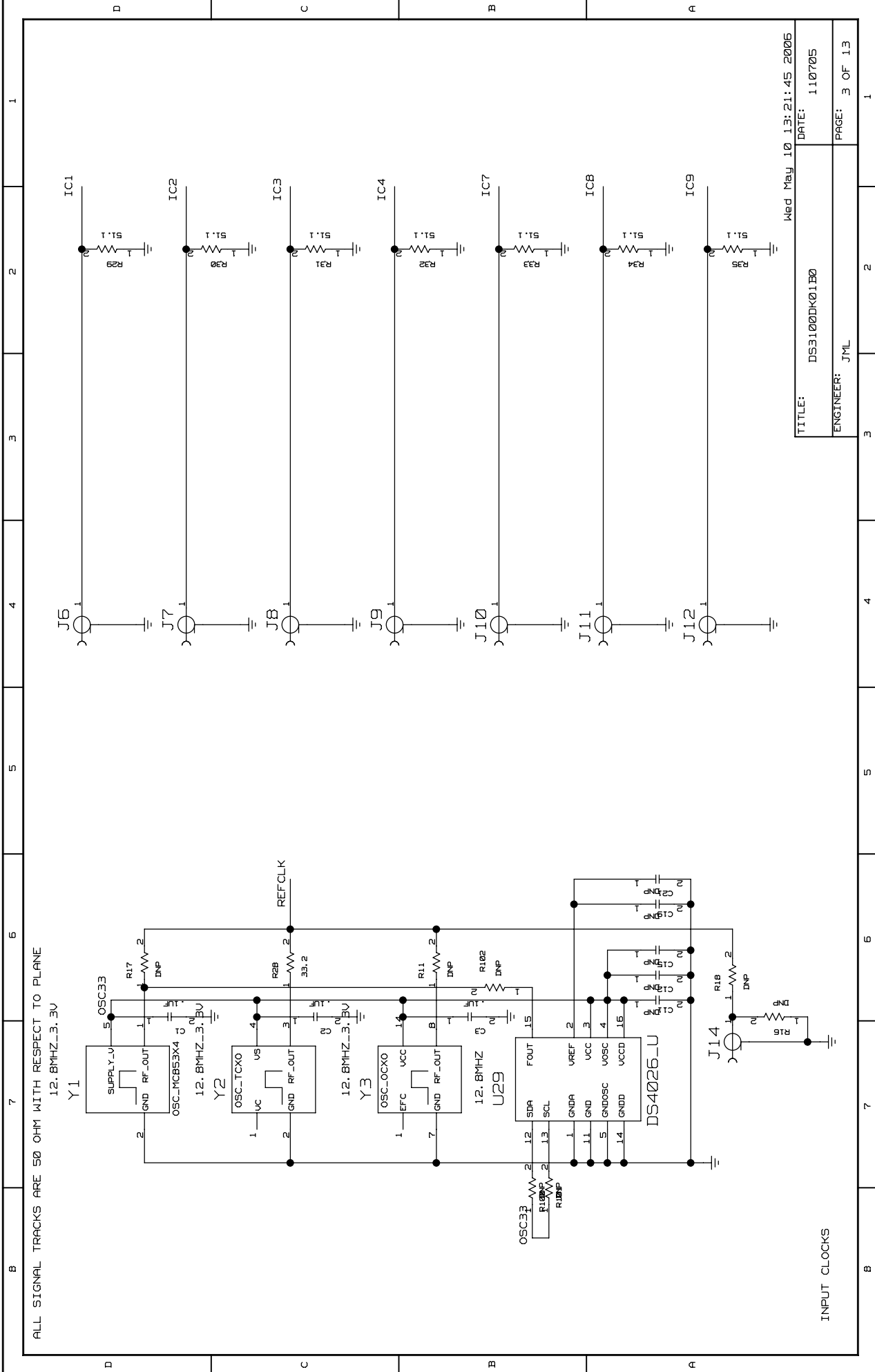
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DATE: 110705

ENGINEER: JML

PAGE: 2 OF 13



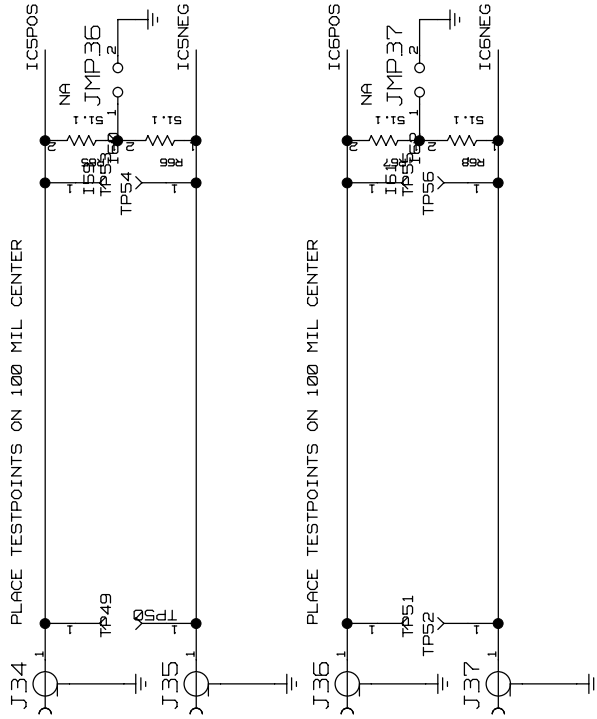
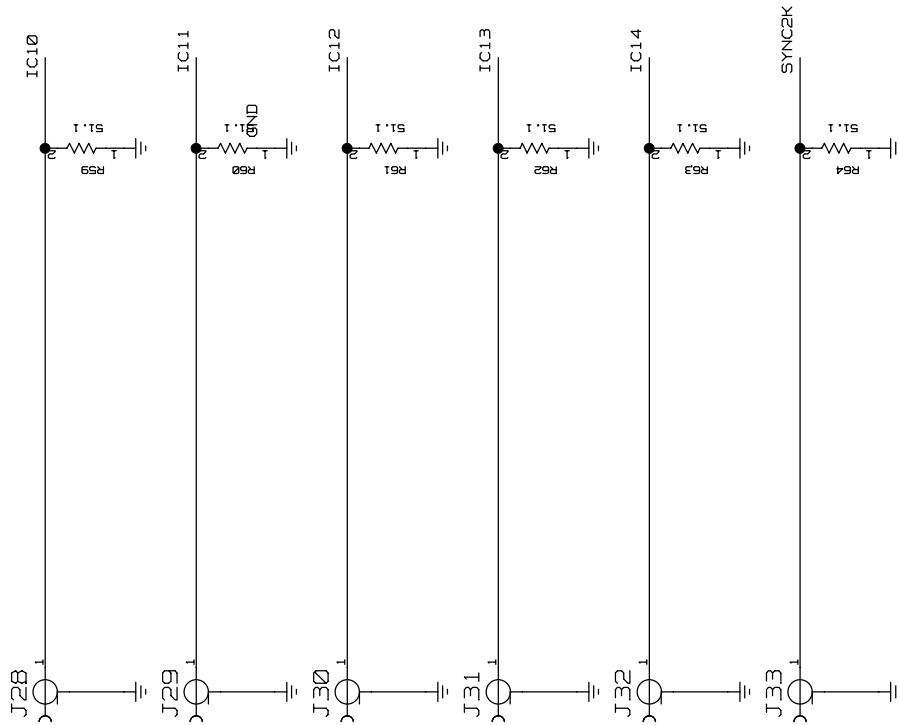
ALL SIGNAL TRACKS ARE 50 OHM WITH RESPECT TO PLANE 12.8MHZ_3.3V

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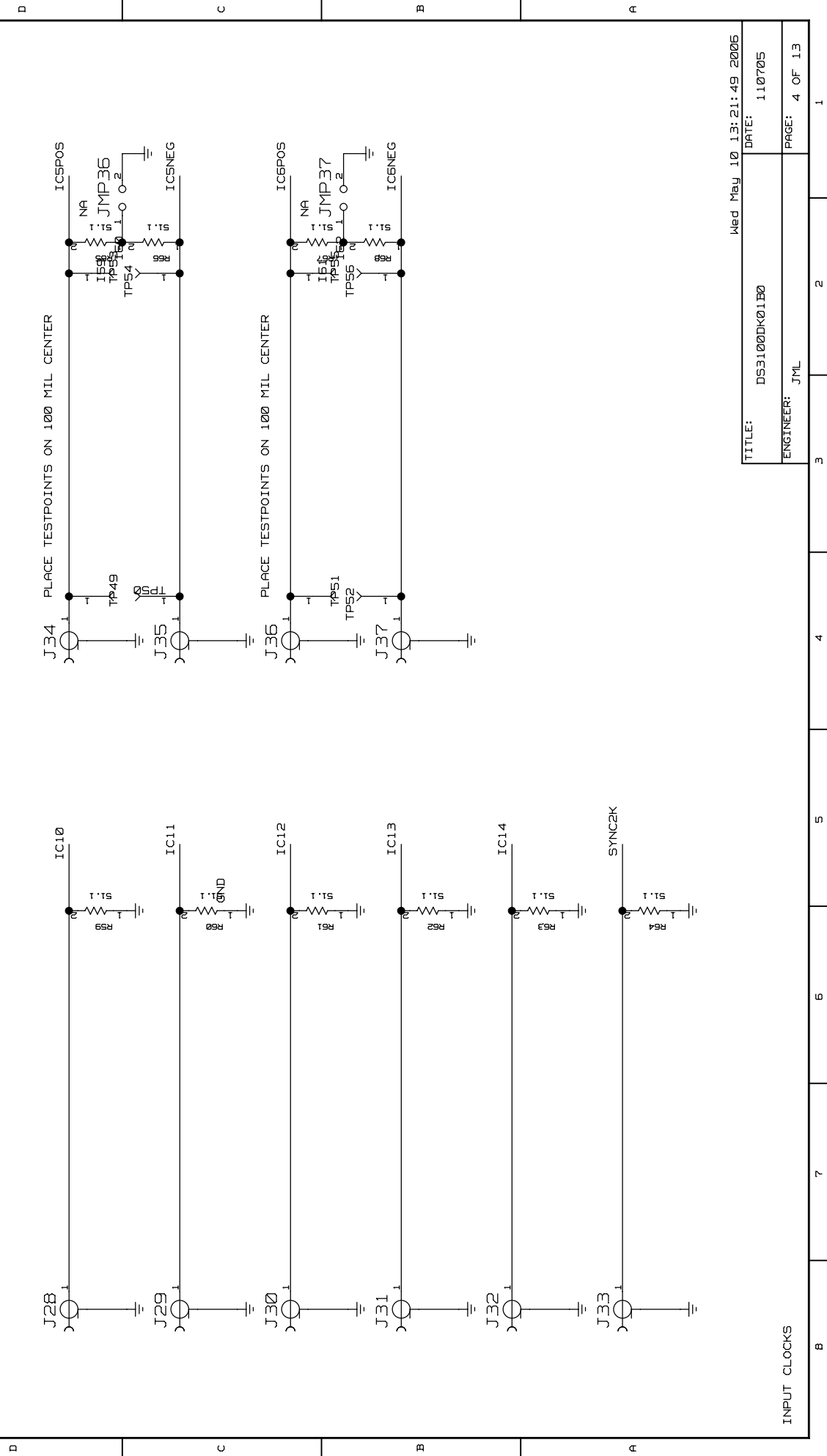
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INPUT CLOCKS

ALL SIGNAL TRACKS ARE 50 OHM WITH RESPECT TO PLANE



B 7 6 5 4 3 2 1

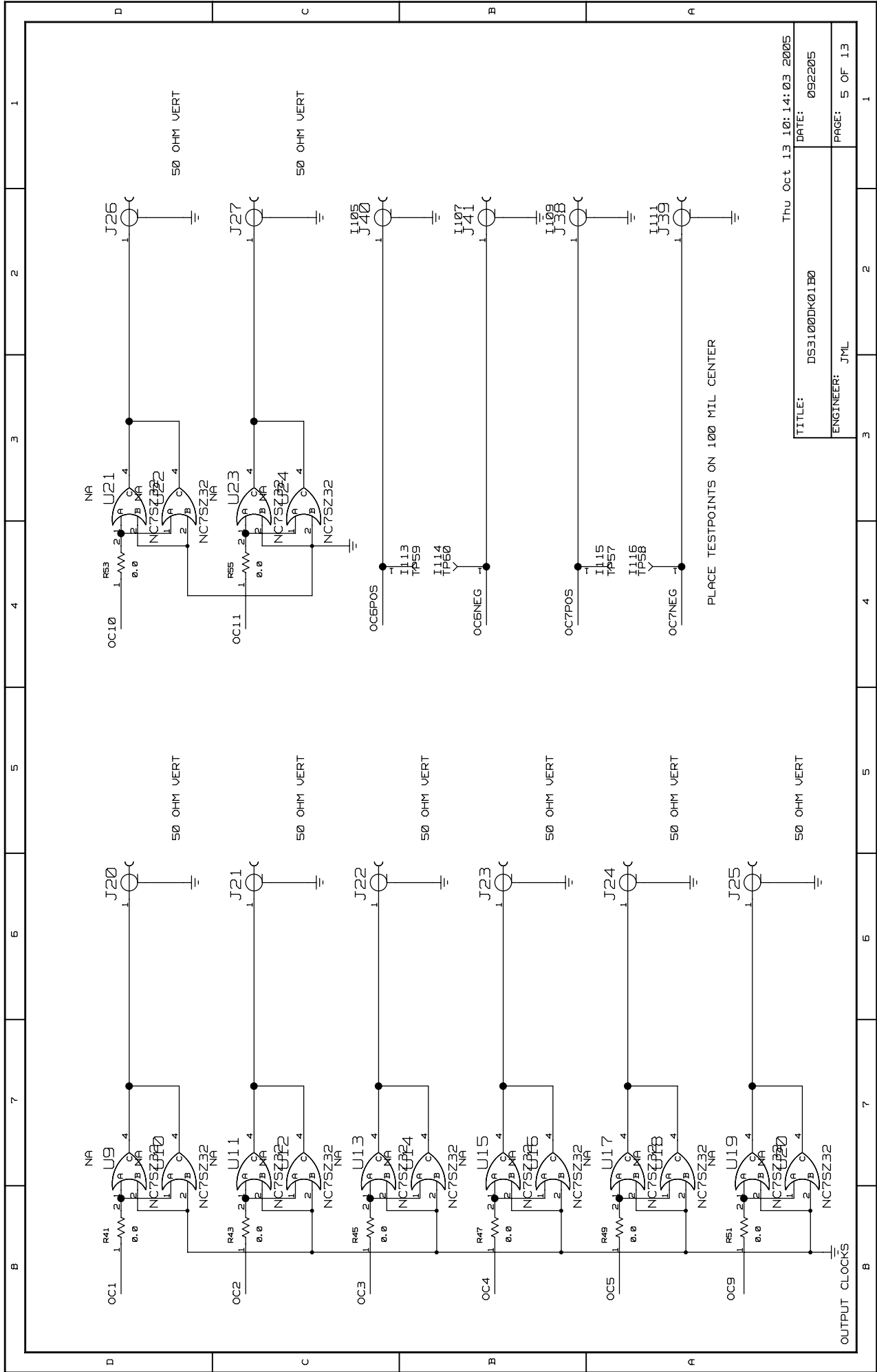


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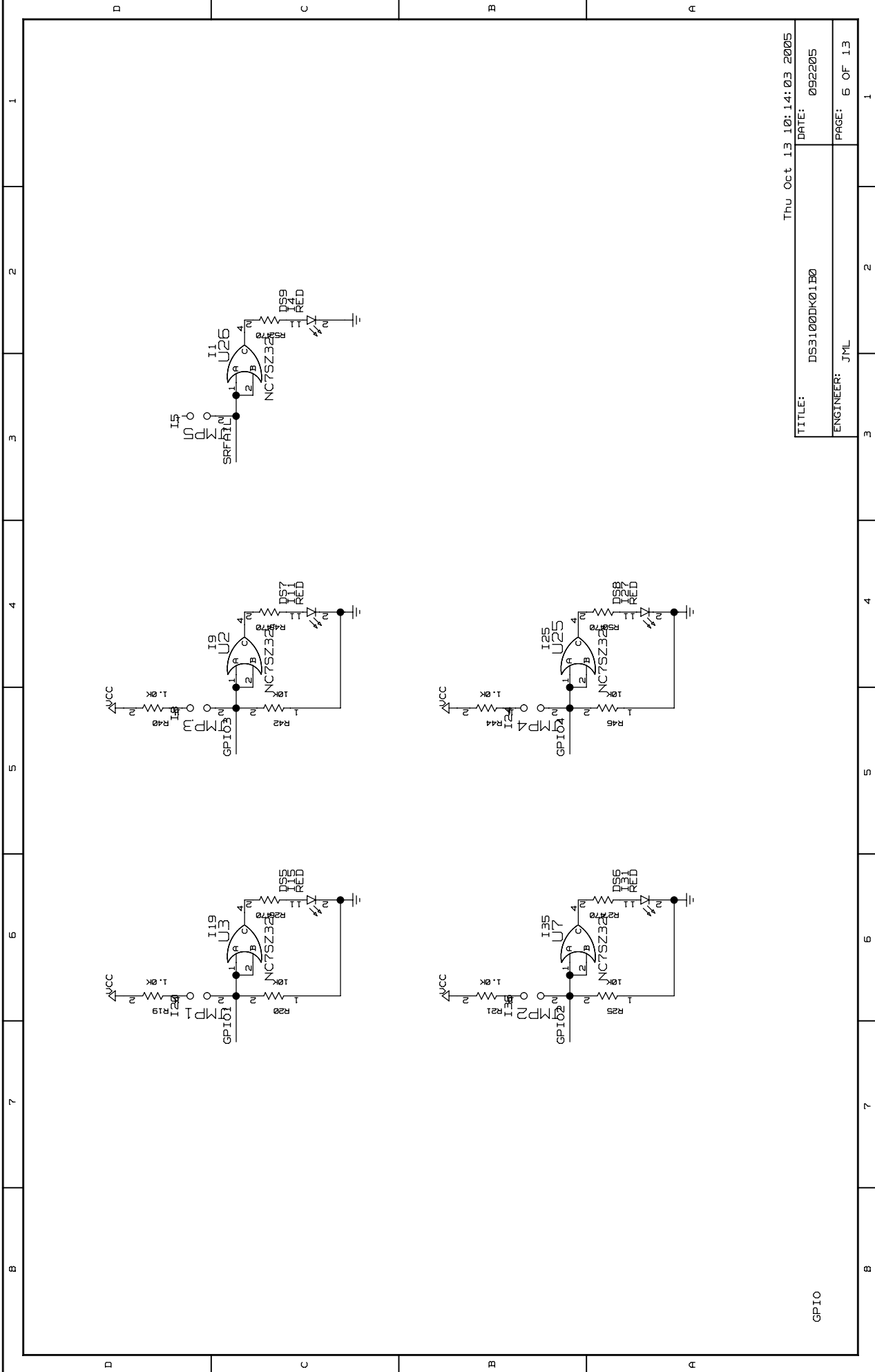
INPUT CLOCKS

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 PAGE: 5 OF 13



GPIO

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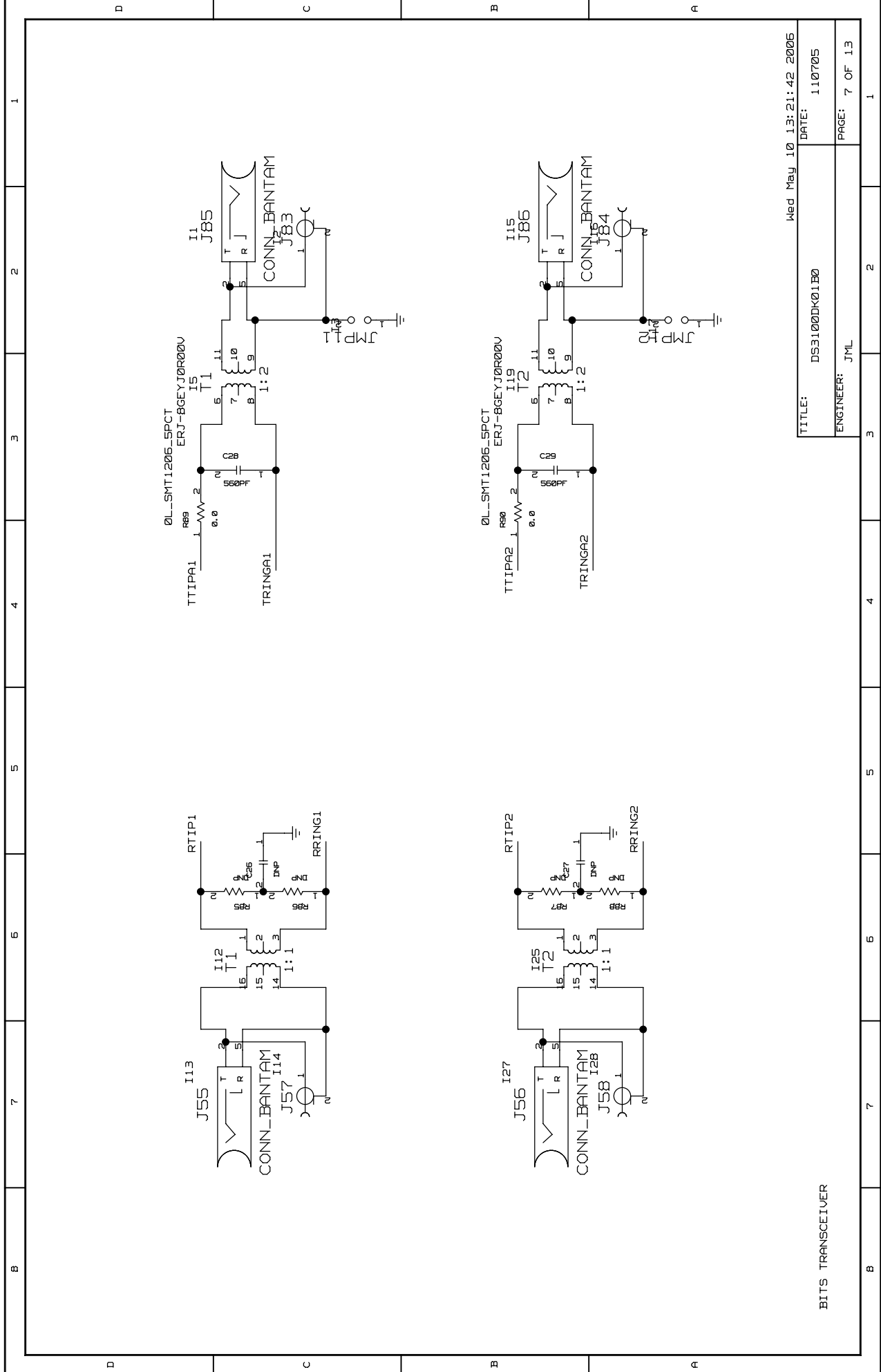
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PAGE: 6 OF 13

B 1 2 3 4 5 6 7

D C B A 1 2 3 4 5 6 7

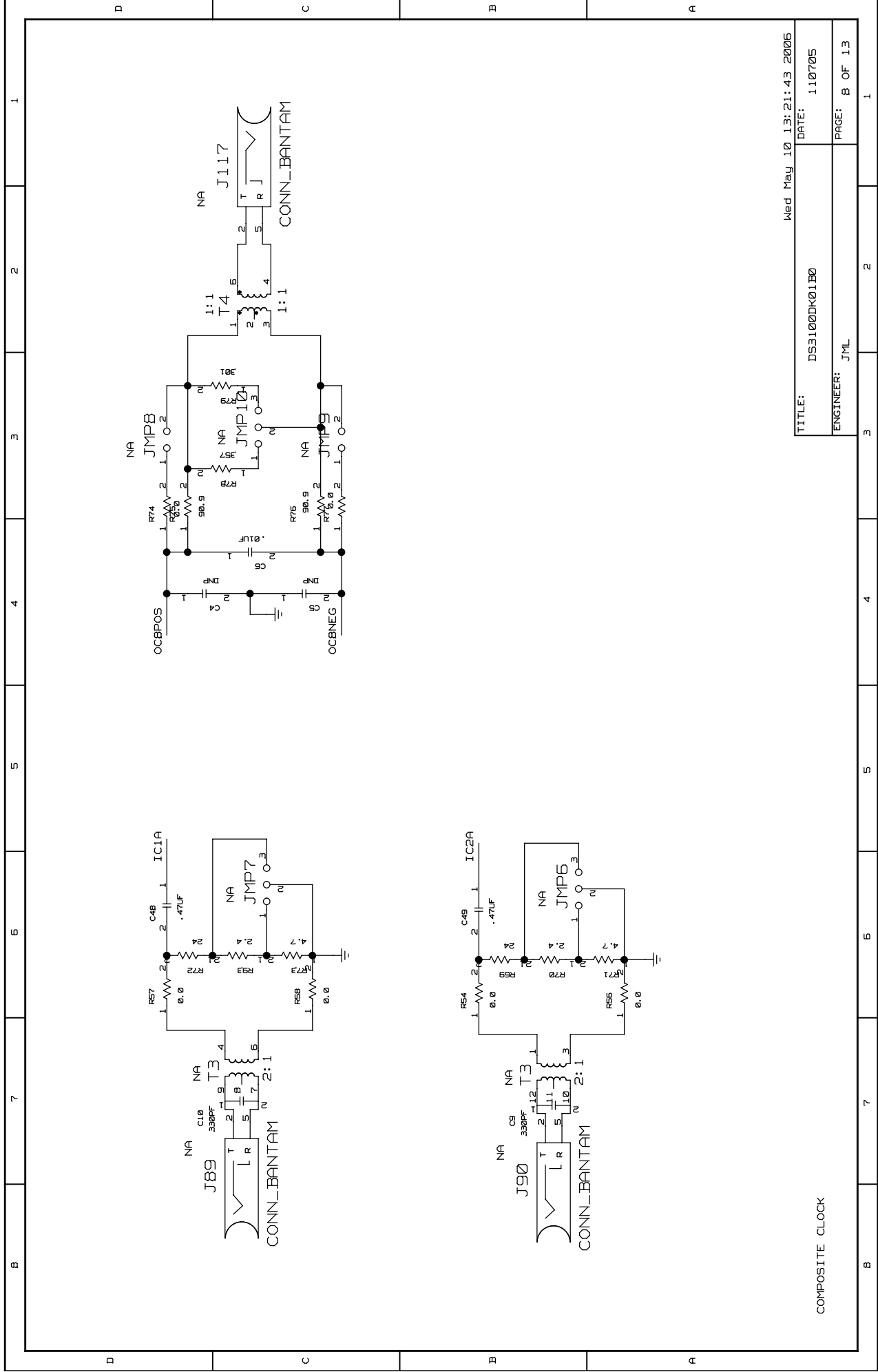


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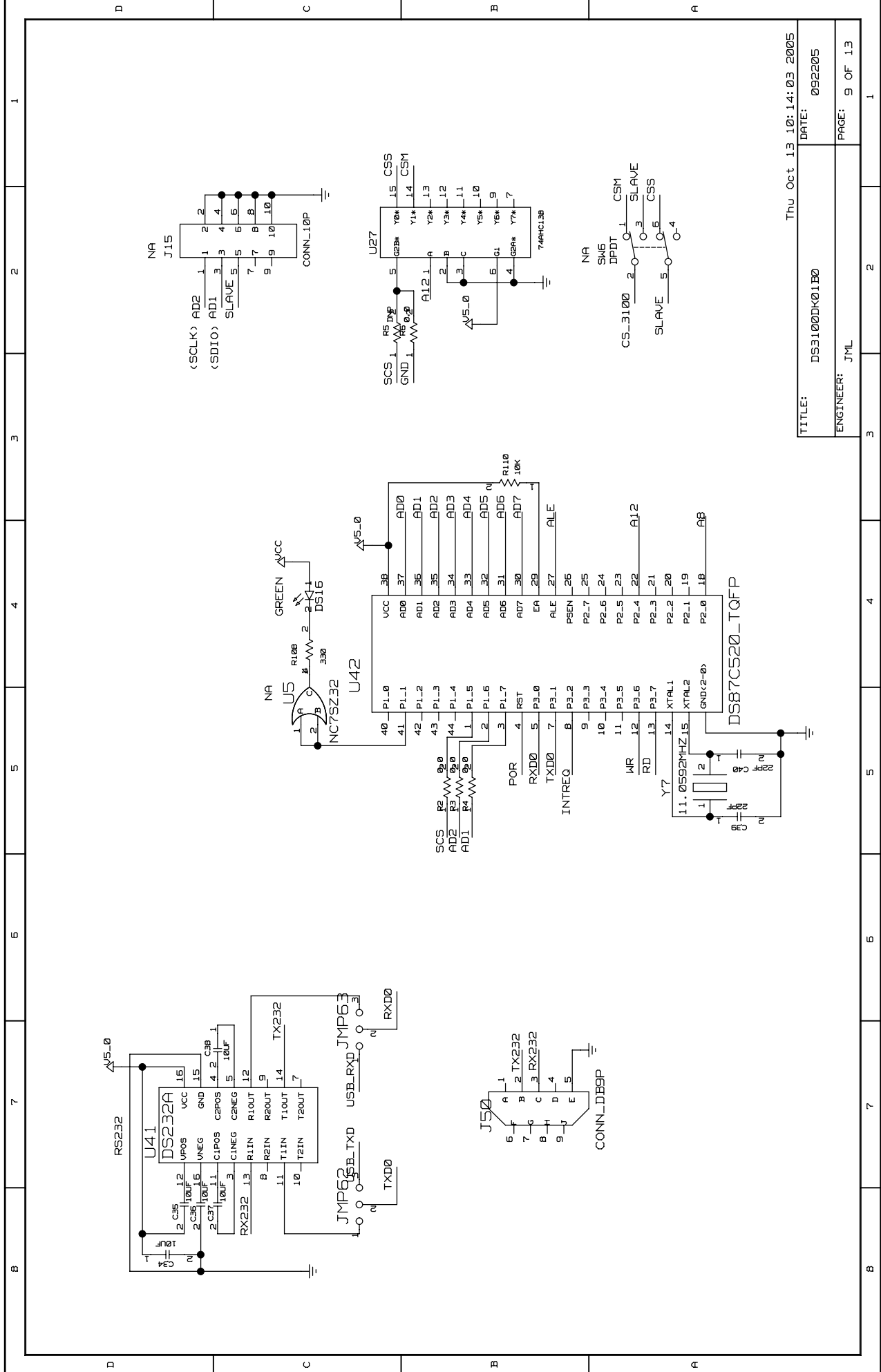
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 PAGE: 7 OF 13

Wed May 10 13:21:42 2006

BITS TRANSCEIVER

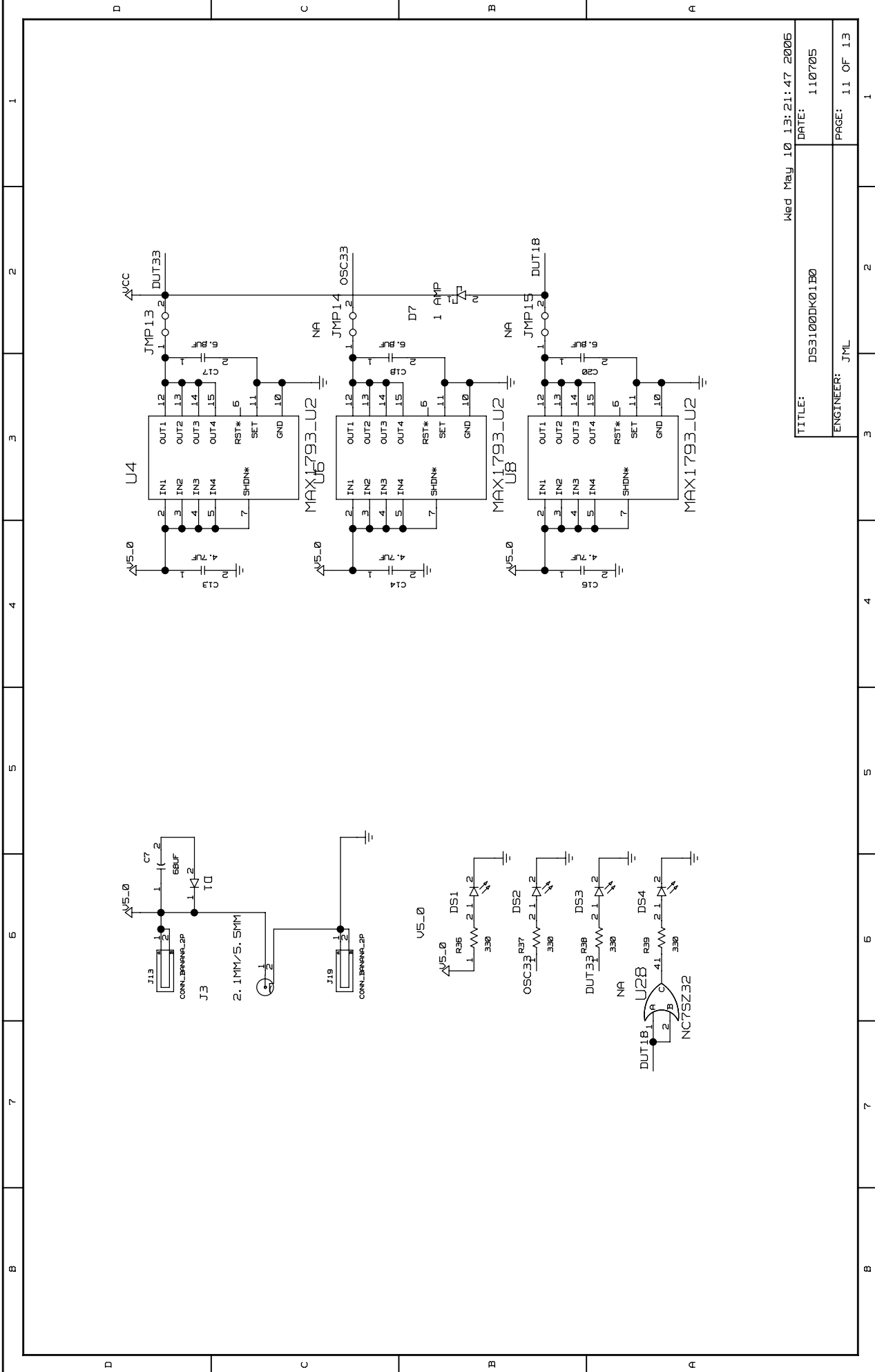


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ENGINEER:	JML	PAGE:	B OF 13



Thu Oct 13 10:14:03 2005
 TITLE: DS3100K01B0
 DATE: 092205
 ENGINEER: JML
 PAGE: 9 OF 13

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



Wed May 10 13:21:47 2006

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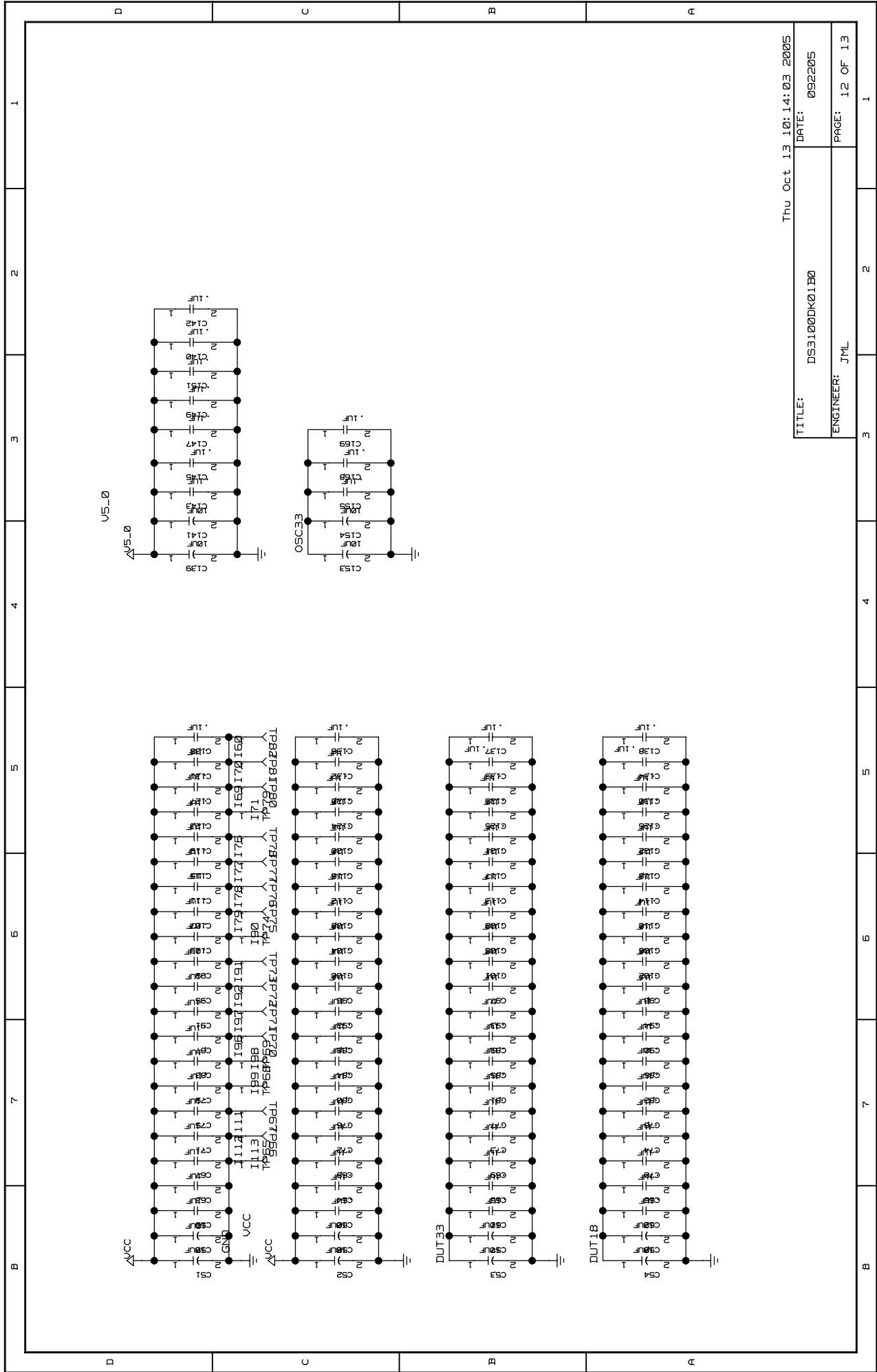
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B 7 6 5 4 3 2 1

B 7 6 5 4 3 2 1

D C B A

D C B A



Thu Oct 13 10:14:03 2005

DATE: 092205

TITLE: DS3100DK01B0

ENGINEER: JML

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D	<p style="text-align: center;">REVISION HISTORY -</p> <table border="0"> <tr> <td style="vertical-align: top;">01 -</td> <td style="vertical-align: top;">110705 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">RELEASE FOR REVIEW</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">02 -</td> <td style="vertical-align: top;">111905 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">FIX TRANSFORMER ISSUES, ADDED POWER JACK, FIXED CSM/CSS LOGIC, ADDED TPS</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">03 -</td> <td style="vertical-align: top;">112105 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">MOVED MEMORY MAP, OTHER MISCELLANEOUS</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">04 -</td> <td style="vertical-align: top;">010405 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">CHANGED REF DESIGNATORS TO MATCH EE</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">05 -</td> <td style="vertical-align: top;">011305 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">REMOVED 5V CAPS, LEDS AND SWITCHES FROM MICRO, LOW Z TP FROM ICN</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">A0 -</td> <td style="vertical-align: top;">012105 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;">RELEASE TO FAB</td> <td colspan="4"></td> </tr> <tr> <td style="vertical-align: top;">B0 -</td> <td style="vertical-align: top;">050205 -</td> <td style="vertical-align: top;">-</td> <td style="vertical-align: top;"> ADDED BUFFER TO 1.8V LED ADDED 0 OHM RESISTORS AT SDIO, SCLK, SCS ADDED INTEL BUS CONNECTIONS MADE INTEL MUX MODE DEFAULT ADDED 330PF CAPS AT COMPOSITE CLOCK INPUT FIXED COMPOSITE CLOCK TERMINATION RES CHANGED 138 TO AHC FROM HC MOVED UP OK LED TO P1.1 AND REVERSED LOGIC CHANGED CAP ON COMPOSITE CLOCK TX TO .01UF ADDED SHORTED JUMPERS AT REGULATORS FOR ACCESS MOVED CSM TO 1000 AND CSS TO 0 ADDED DS4026 TCXO AND SUPPORTING COMPONENTS </td> <td colspan="4"></td> </tr> </table>							01 -	110705 -	-	RELEASE FOR REVIEW					02 -	111905 -	-	FIX TRANSFORMER ISSUES, ADDED POWER JACK, FIXED CSM/CSS LOGIC, ADDED TPS					03 -	112105 -	-	MOVED MEMORY MAP, OTHER MISCELLANEOUS					04 -	010405 -	-	CHANGED REF DESIGNATORS TO MATCH EE					05 -	011305 -	-	REMOVED 5V CAPS, LEDS AND SWITCHES FROM MICRO, LOW Z TP FROM ICN					A0 -	012105 -	-	RELEASE TO FAB					B0 -	050205 -	-	ADDED BUFFER TO 1.8V LED ADDED 0 OHM RESISTORS AT SDIO, SCLK, SCS ADDED INTEL BUS CONNECTIONS MADE INTEL MUX MODE DEFAULT ADDED 330PF CAPS AT COMPOSITE CLOCK INPUT FIXED COMPOSITE CLOCK TERMINATION RES CHANGED 138 TO AHC FROM HC MOVED UP OK LED TO P1.1 AND REVERSED LOGIC CHANGED CAP ON COMPOSITE CLOCK TX TO .01UF ADDED SHORTED JUMPERS AT REGULATORS FOR ACCESS MOVED CSM TO 1000 AND CSS TO 0 ADDED DS4026 TCXO AND SUPPORTING COMPONENTS					A
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